#3/Elections 1/22/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

HOSHINO, Masataka

Serial No.: **09/982,963**

Filed: **October 22, 2001**

Group Art Unit: 2823

Examiner: **William D. Coleman**

P.T.O. Confirmation No.: 8557

For: **THREE DIMENSIONAL SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR MAKING THE SAME**

RESPONSE TO THE RESTRICTION REQUIREMENT

Commissioner for Patents
Washington, D.C. 20231

Date: January 17, 2003

Sir:

This is in response to the Office Action of December 18, 2002, requiring restriction between two alleged inventions under the provisions of 35 USC § 121.

In the Action, the examiner made a restriction requirement between the inventions of **Group I** drawn to a semiconductor device (claims 1-8); and **Group II** drawn to a method of manufacturing a semiconductor device (claims 9-15).

Applicants hereby provisionally elect **Group I, that is, claims 1-8,** for examination on the merits in this application. Applicants reserve the right to file one or more divisional applications directed to the subject matter of the non-elected claims.

Favorable consideration of the subject application is respectfully requested.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this response.

Respectfully submitted,

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Dwh/nk

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